Wednesday July 13, 2011

07:30 – 09:00: Symposium Registration

09:00 – 10:00: Opening Session

09:00 – 09:15: Welcome Message
M.Nicolaidis (TIMA Lab), A.Paschalis (U Athens), General Chairs
D.Gizopoulos (U Athens), X.Vera (Intel Barcelona Research Center), Program Chairs

09:15 – 10:00: Keynote Talk
Prof. Babak Falsafi (EPFL)

10:00 – 10:15: Break

10:15 – 11:15: Session 1 – Degradation Modeling and Transients Tolerance

1. Modeling and Mitigating NBTI in Nanoscaled Circuits, S.Khan, S.Hamdioui (TU Delft)
2. RVC-Based Time-Predictable Faulty Caches for Safety-Critical Systems, J.Abella, E.Quirones, F.Cazorla, M.Valero (Barcelona Supercomputing Center), Y.Sazeides (U Cyprus)
3. Towards Functional-Safe Timing-Dependable Real-Time Architectures, M.Paoliier (Barcelona Supercomputing Center), R.Mariani (YOGITECH)

11:15 – 11:30: Coffee Break

11:30 – 12:30: Session 2 – Faults in Real-Time Systems

1. An Intellectual Property Core to Detect Task Scheduling-Related Faults in RTOS-Based Embedded Systems, D.Silva, L.Bozani, F.Vargas (Catholic University - PUCRS)
3. Selective Fault Tolerance for Finite State Machines, M.Augustin (BTU Cottbus), M.Goessel (U Potsdam), R.Kraemer (IHP)

12:30 – 13:30: Lunch

13:30 – 14:30: Session 3 – Fault Tolerance

2. Selective Fault Tolerance for Finite State Machines, M.Augustin (BTU Cottbus), M.Goessel (U Potsdam), R.Kraemer (IHP)
3. A New IP Core for Fast Error Detection and Fault Tolerance in COTS-based Solid State Mass Memories, E.Costenaro, M.Violante (Politecnico di Torino), D.Alexandrescu (iRoC)

14:30 – 14:45: Break

14:45 – 15:45: Session 4 – Variability and Degradation Tolerance in Multicores

1. Variability-aware Task Mapping Strategies for Many-core Processor Chips, F.Chaix, G.Bizot, M.Nicolaidis, N.Zergainoh (TIMA Laboratory)
2. On Graceful Degradation of Microprocessors in Presence of Faults via Resource Banking, R.Rodrigues, S.Kundu (U Massachusetts at Amherst)

15:45 – 16:00: Coffee Break

16:00 – 17:00: Session 5 – Memory BIST

1. A Multi-Objective Optimization for Memory BIST Sharing using a Genetic Algorithm, Y.Kieffer (G-Scop Lab), L.Zaourar (LIPS Lab), A.Wenzel (ST)

17:00 – 17:15: Break

17:15 – 18:15: Session 6 – Reliability Evaluation

1. A Reliable Fault Classifier for Dependable Systems on SRAM-based FPGAs, C.Sandionigi, C.Bolchini (Politecnico di Milano)
3. Estimation of Component Criticality in Early Design Steps, M.Sauer (U Freiburg), A.Czutro (U Freiburg), I.Polian (U Passau), B.Becker (U Freiburg)

18:15 – 18:30: Break

18:30 – 19:30: Special Session 1 – New Reliability Mechanisms in Memory Design for sub-22nm Technologies

Thursday July 14, 2011

09:00 – 10:00: Session 7 – Testing and Error Tolerance for Low Power

2. Internal Model Control for a Self-Tuning Delay-Locked Loop in UWB Communication Systems, R.Alhakim (TIMA Lab), E.Simeu (TIMA Lab), R.Kraemer (IHP)
3. Real Time Cross-Layer Adaptation for Minimum Energy Wireless Image Transport using Bit Error Rate Control, J.Natarajan, S.Sen, A.Chatterjee (Georgia Institute of Technology)

10:00 – 10:15: Break

10:15 – 11:15: Special Session 2 – Security Concerns in Modern Integrated Circuits

Organizer: Y.Makris (Yale U) Moderators: Y.Makris (Yale U), A.Veneris (U Toronto)
S2.1 The Cost of Cryptography in Hardware, I.Verbaumwede, K. U. Leuven
S2.2 Countermeasures against Fault Attacks: the Good, the Bad, and the Ugly, P.Maistri, R.Leveugle, TIMA Laboratory
S2.3 The Rise of Hardware Trojans, B.Sunar, Worcester Polytechnic Institute

11:15 – 11:30: Coffee Break

11:30 – 12:30: Session 8 – Error Tolerant SRAM Designs

8.1 A Novel Radiation Tolerant SRAM Design Based on Synergistic Functional Component Separation for Nanoscale CMOS, Y.Shiyanovskii, A.Rajendran, C.Papachristou (Case Western Reserve U)
8.2 Noise Margin, Critical Charge and Power-Delay Tradeoffs for SRAM Design Space Exploration, A Rajendran, Y.Shiyanovskii, F.Wolff, C.Papachristou (Case Western Reserve U)
8.3 Multiple-Bit-Upset and Single-Bit-Upset Resilient SRAM Bitcell Layout with Divided Wordline Structure, S.Yoshimoto (Kobe U), T.Amashtia (Kobe U), D.Kozuwa (Kyushu U),